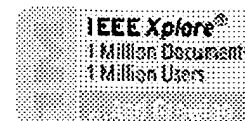




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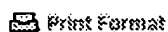
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**1 The K-pulse concept**

*Kennaugh, E.;*

Antennas and Propagation, IEEE Transactions on [legacy, pre - 1988] , Volume: 29 , Issue: 2 , Mar 1981

Pages:327 - 331

[\[Abstract\]](#)   [\[PDF Full-Text \(488 KB\)\]](#)   **IEEE JNL**

**2 Register transfer level power optimization with emphasis on glitch analysis and reduction**

*Raghunathan, A.; Dey, S.; Jha, N.K.;*

Computer-Aided Design of Integrated Circuits and Systems, IEEE Transactions on , Volume: 18 , Issue: 8 , Aug. 1999

Pages:1114 - 1131

[\[Abstract\]](#)   [\[PDF Full-Text \(340 KB\)\]](#)   **IEEE JNL**

**3 On the functional validity of the worm-killing worm**

*Hyogen Kim; Inhye Kang;*

Communications, 2004 IEEE International Conference on , Volume: 4 , 20-24 June 2004

Pages:1902 - 1906 Vol.4

[\[Abstract\]](#)   [\[PDF Full-Text \(399 KB\)\]](#)   **IEEE CNF**

**4 Optical diagnostics of shock waves generated by a pulsed streamer discharge in water**

*Hemmert, D.; Shiraki, K.; Yokoyama, T.; Katsuki, S.; Bluhm, H.; Akiyama, H.;*

Pulsed Power Conference, 2003. Digest of Technical Papers. PPC-2003. 14th IEEE International , Volume: 1 , 15-18 June 2003

Pages:232 - 235 Vol.1

[\[Abstract\]](#)   [\[PDF Full-Text \(513 KB\)\]](#)   **IEEE CNF**



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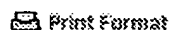
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*Kuo, J.B.; Liao, H.J.; Chen, H.P.;*

Electronics Letters, Volume: 28, Issue: 5, 27 Feb. 1992

Pages:476 - 477

[\[Abstract\]](#)   [\[PDF Full-Text \(180 KB\)\]](#)   IEEE JNL

### 2 Variants of an improved carry look-ahead adder

*Doran, R.W.;*

Computers, IEEE Transactions on, Volume: 37, Issue: 9, Sept. 1988

Pages:1110 - 1113

[\[Abstract\]](#)   [\[PDF Full-Text \(196 KB\)\]](#)   IEEE JNL

### 3 Design of compact static CMOS carry look-ahead adder using recursive output property

*Lee, Y.T.; Park, I.C.; Kyung, C.M.;*

Electronics Letters, Volume: 29, Issue: 9, 29 April 1993

Pages:794 - 796

[\[Abstract\]](#)   [\[PDF Full-Text \(220 KB\)\]](#)   IEEE JNL

### 4 On the adders with minimum tests

*Kajihara, S.; Sasao, T.;*

Test Symposium, 1997. (ATS '97) Proceedings., Sixth Asian, 17-19 Nov. 1997

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[\[Abstract\]](#)   [\[PDF Full-Text \(396 KB\)\]](#)   IEEE CNF

### 5 Evaluation of three 32-bit CMOS adders in DCVS logic for self-timed circuits

*Ruiz, G.A.;*

Solid-State Circuits, IEEE Journal of, Volume: 33, Issue: 4, April 1998

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